CLAIMS:

1. An integrated circuit comprising:

a memory including:

an array of transistors formed within a first well of a single-crystal semiconductor region of a substrate;

a plurality of storage cells each including an access transistor, said access transistor being a transistor of said array of transistors;

a plurality of bitlines, each said bitline coupled to the access transistors of respective storage cells of said plurality of storage cells; and

a multiplexer including a first select transistor and a second select transistor of a plurality of select transistors, said plurality of select transistors being transistors of said array of transistors, said first select transistor being operable to select a first bitline of said plurality of bitlines to couple to a signal line, and said second select transistor being operable to select a second bitline of said plurality of bitlines to couple to said signal line.

2. The integrated circuit of claim 1 wherein said substrate has a main surface extending in a first horizontal direction and in a second horizontal direction transverse to said first horizontal direction, and wherein each said transistor of said array of transistors has a conduction channel which is oriented in a vertical direction substantially perpendicular to said first horizontal direction and said second horizontal direction.

3. The integrated circuit of claim 1 wherein said substrate has a main surface extending in a first horizontal direction

and in a second horizontal direction transverse to said first horizontal direction, wherein said plurality of bitlines extend generally in said first horizontal direction and wherein each of said multiplexers further includes a plurality of conductors extending in said second horizontal direction, said plurality of conductors including a first conductor coupled to operate said first select transistor and a second conductor coupled to operate said second select transistor.

4. The integrated circuit of claim 3 wherein each of said plurality of conductors comprises a layer of polycrystalline silicon.

5. The integrated circuit of claim 4 wherein each said select transistor of said array of transistors has a conduction channel which is oriented in a vertical direction substantially perpendicular to said first horizontal direction and said second horizontal direction.

6. The integrated circuit of claim 5 wherein said signal line comprises a master bitline operable to conduct a signal between said bitline selected by said multiplexer and a sense amplifier.

7. The integrated circuit of claim 6 wherein said first select transistor and said second select transistor are conductively coupled to a first diffusion region of said single crystal semiconductor region and wherein said master bitline conductively contacts said first diffusion region.

8. The integrated circuit of claim 7 wherein said master bitline conductively contacts said first diffusion region in an area between conductors of said plurality of conductors.

9. The integrated circuit of claim 8 wherein said first select transistor includes a left transistor having a vertically oriented conduction channel and a right transistor having a vertically oriented conduction channel, said left transistor and said right transistor being coupled in series and being operable by said first conductor to select said first bitline to couple to the master bitline.

10. The integrated circuit of claim 9 wherein a drain region of said left transistor is conductively coupled to said first bitline, and a drain region of said right transistor is conductively coupled to said master bitline through said first diffusion region.

11. The integrated circuit of claim 10 wherein source regions of said left transistor and said right transistor are coupled together to a capacitor.

12. A method of operating a memory of an integrated circuit comprising:

providing a memory including:

an array of transistors formed within a first well of a single-crystal semiconductor region of a substrate, said array of transistors including first and second select transistors;

a plurality of storage cells each including an access transistor, said access transistor being a transistor of said array of transistors;

a plurality of bitlines including a first bitline and a second bitline, each said bitline coupled to the access transistors of respective storage cells of said plurality of storage cells;

operating said first select transistor to connect said first bitline to a master bitline; and

operating said second select transistor to connect said second bitline to a master bitline.

13. The method of claim 12 wherein said substrate has a main surface extending in a first horizontal direction and in a second horizontal direction transverse to said first horizontal direction, and wherein each said select transistor of said array of transistors has a conduction channel which is oriented in a vertical direction substantially perpendicular to said first horizontal direction and said second horizontal direction.

14. The method of claim 12 wherein said substrate has a main surface extending in a first horizontal direction and in a second horizontal direction transverse to said first horizontal direction, wherein said plurality of bitlines extend generally in said first horizontal direction and said first and second select transistors are operated by first and second conductors, respectively, said first and second conductors extending in said second horizontal direction.

15. The method of claim 14 wherein said first and second conductors comprises a layer of polycrystalline silicon.

16. The method of claim 15 wherein each of said first and second select transistors has a conduction channel which is

oriented in a vertical direction substantially perpendicular to said first horizontal direction and said second horizontal direction.

17. The method of claim 16 further comprising conducting a signal on said master bitline between a selected bitline of said first bitline and said second bitline and a sense amplifier.

18. The method of claim 17 wherein said first and said second select transistors are connected by a first diffusion region of said single crystal semiconductor region to said master bitline.

19. The method of claim 18 wherein said master bitline conductively contacts said first diffusion region in an area between said first and said second conductors.

20. The method of claim 14 wherein said first select transistor includes a left transistor having a vertically oriented conduction channel and a right transistor having a vertically oriented conduction channel, said left transistor and said right transistor being coupled in series and being operable by said first conductor to select said first bitline to couple to the master bitline.